Datasheet: SENIS® SENCS1De

High Speed High Accuracy Current Sensor IC

1. DESCRIPTION

The SENIS® SENCS1De is a programmable current sensor that uses a combination of linear Hall sensor and Coil to increase the measurement bandwidth and to improve the signal-to-noise ratio, i.e. to increase resolution. This combination allows the highest frequency bandwidth of this kind of sensor on the market. The sensor provides and analog output voltage proportional to the applied magnetic field density.
The transfer characteristic of the sensor is factory trimmed over temperature and is programmable (offset, sensitivity, filtering...) during end-of-line customer calibration beyond the default factory trimming.
In a typical current sensing application, the sensor is used in a combination with a ring shaped soft ferromagnetic core. This core is recommended to be ferrite or laminated for high bandwidth applications.

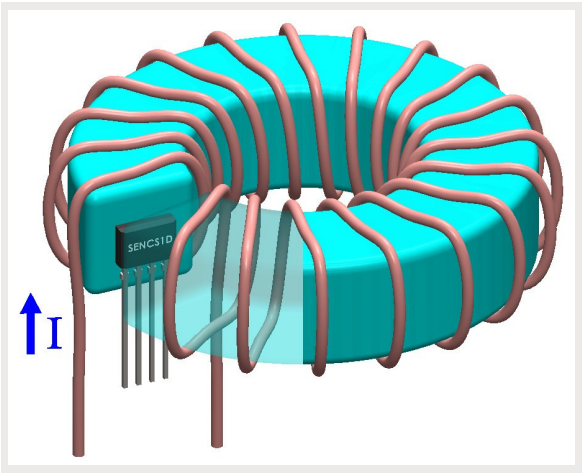

Figure 1: *SENCS1De application*

KEY FEATURES:

- Wide power supply range 3.3V - 5.5V
- Selectable measurement ranges from 5 mT up to even 1 T
- High speed AC and DC current sensing with 1 MHz bandwidth and response time <1 µs
- Selectable ratiometric analog output
- Low noise 25 µTrms
- OTP memory with 4 pages for user settings
- Programmable quiescent reference output 0-5V
- Single wire serial interface (Manchester protocol) for sensor configuration
- Operating temperature : -40 /+125°C
- Protection circuit for 12V surge
- ESD: 4KV
- Under/Over voltage detection

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3. TYPICAL APPLICATIONS

Smart fuse overcurrent detection
- Smart battery junction boxes and battery management system
- DC-DC and AC/DC converter
- BLCD motor current monitoring
- Core-based and coreless sensor applications

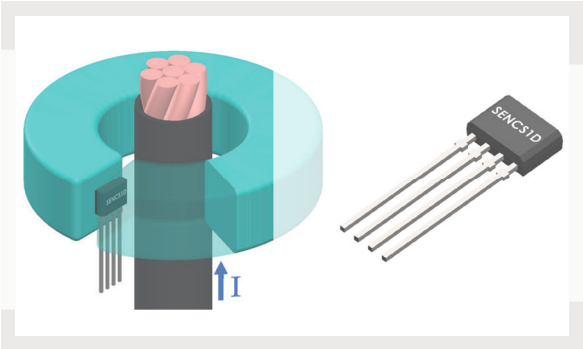


Figure 2: *Core-based sensor applications*

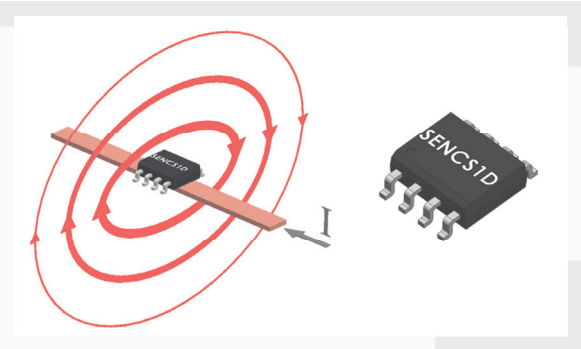


Figure 3: *Coreless sensor applications*

4. BLOCK DIAGRAM

Figure 4 shows the block diagram of the sensor chip with horizontal and vertical Hall element (hHe and vHe) as well as the corresponding horizontal and vertical coil. Note that the vertical coil is discrete and is therefore placed off-chip.

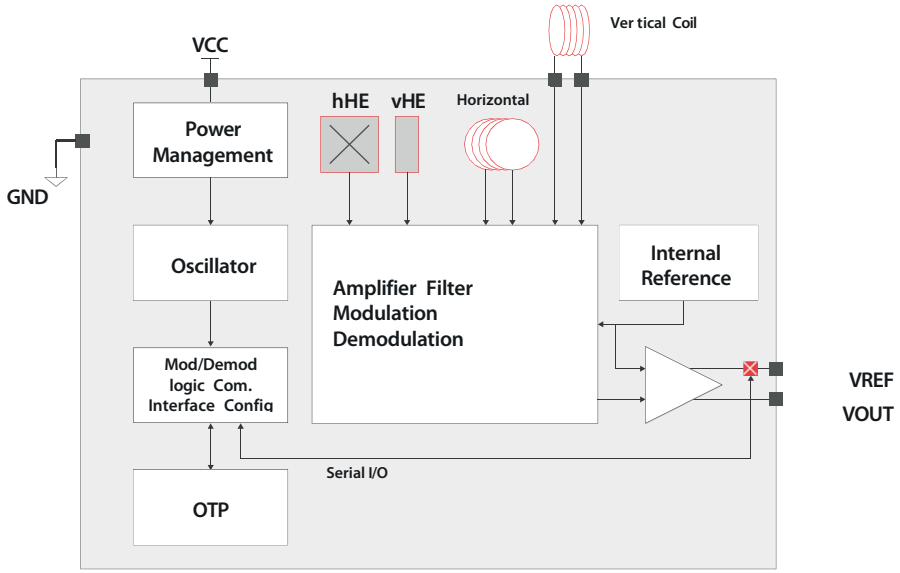
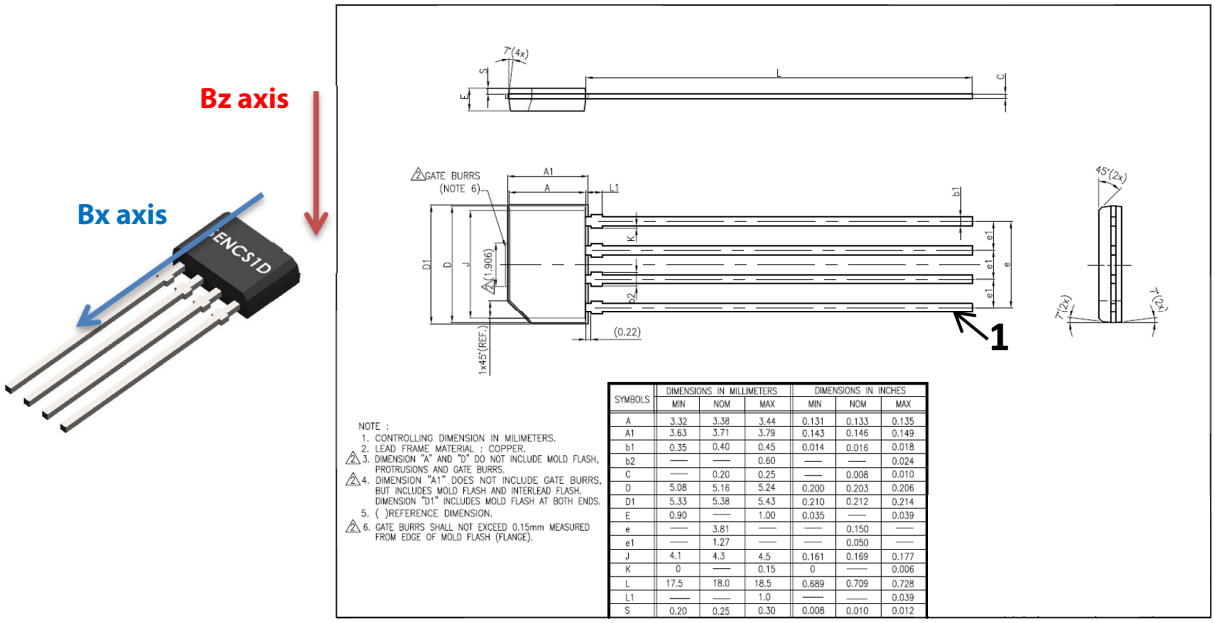


Figure 4: *Block diagram of SENCS1De*

5. PACKAGE INFORMATION AND ORDERING:

The non-magnetic SIP-4L package. The field sensitive volume (FSV) is about 0.75 mm below the surface of the package. Contact SENIS for details.

5.1. Dimensions



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.32	3.38	3.44	0.131	0.133	0.135
A1	3.63	3.71	3.79	0.143	0.146	0.149
b1	0.35	0.40	0.45	0.014	0.016	0.018
b2	——	——	0.60	——	——	0.024
C	——	0.20	0.25	——	0.008	0.010
D	5.08	5.16	5.24	0.200	0.203	0.206
D1	5.33	5.38	5.43	0.210	0.212	0.214
E	0.90	——	1.00	0.035	——	0.039
e	——	3.81	——	——	0.150	——
e1	——	1.27	——	——	0.050	——
J	4.1	4.3	4.5	0.161	0.169	0.177
K	0	——	0.15	0	——	0.006
L	17.5	18.0	18.5	0.689	0.709	0.728
L1	——	——	1.0	——	——	0.039
S	0.20	0.25	0.30	0.008	0.010	0.012

Figure 5: *Package information; Dimensions SIP-4L-lead package. The field sensitive volume (FSV) is located at the center of the package. Drawings are not to scale.*

TABLE 1: Pin list and function

Pin #	Symbol	Type	Function
1	VCC	POWER	Main power supply (from 3.3V to 5V)
2	VOUT	OUTPUT	Signal output
3	VREF	Output/Input	Quiescent reference output; also used as programming interface; single wire
4	GND	GROUND	Ground

5.2. Ordering

SENCS1De-abc, Explanation for the last three characters in the article name abc:

- a is the package type: 0 = SIP4; 1 = SO-8
- b is the range 1 = 5mT, 2 = 10mT, 3 = 20mT , 4 = 50mT, 5 = 100mT, 6 = 200mT, 7 = 500mT, 8 = 1T
- c is the sensitivity direction: X or Z

6. ABSOLUTE MAXIMUM RATINGS

TABLE 2: Absolute maximal ratings

Parameter	Symbol	Value	Unit
Positive supply voltage	VCC	16	V
Reverse supply voltage		-16	V
Positive Pin voltage		VDD+0.3	V
Output Sourcing Current		50	mA
Output Sinking Current		-50	mA
Storage temperature	TSTG	-50 to 125	°C
Operating ambient temperature	TA	-40 to 125	°C
ESD protection at inputs, HBM	VESD	4	kV

Note that exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7. GLOSSARY OF TERMS

TABLE 3: Glossary of terms

Name, Acronym	Description
BW	Bandwidth (-3 dB)
ESD	Electrostatic Discharge
FSV	Field Sensitive Volume
HBM	Human-Body Model
hHE	horizontal Hall Element; referred to horizontal chip plane (0°)
IC	Integrated Circuit
MSB	Most Significant Bit; e.g. 0b10000000, '1' is the MSB; decimal value 128
NSD	Noise Spectral Density
NVM	Non-Volatile Memory
OTP	One-Time Programmable (Memory)
Ox	Hexadecimal (base 16) number; e.g. decimal 10 equals 0xA
vHE	vertical (90°) Hall Element; referred to horizontal chip plane (0°)
TA	Ambient Temperatur

8. ELECTRICAL CHARACTERISTICS AND SENSOR PERFORMANCE

Unless otherwise noted, the given specifications and characteristics are typical values for VCC=5V and a current consumption of 16 mA.

8.1. General Electrical Specification:

TABLE 4: Typical characteristics related to the power domain

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply voltage	Vcc	3	5	5.5	V
Supply current	Icc		10	15	mA
Vout output Resistance	Rout		5		Ohm
Vref output resistance	Rref		200		Ohm
Power-on reset threshold		2.5		2.7	V
Output capacitive load	Cload		4.7		nF
Output short circuit current	Ishort		100		mA
Output voltage Linear Swing	Vout_sw	0		90	%Vcc
Power-on reset hysteresis			250		mV
Over-voltage threshold		5.0		5.7	V
Over-voltage hysteresis			200		mV
Power-on time			0.4		ms
On chip oscillator	Fosc		20	30	MHz

8.2. Magnetic specifications:

Unless otherwise noted, the presented values are specified for VCC= 5V in the entire operating temperature range (from -40 to 125°C). Ibias=2mA, LPass filter=5kHz, CLK=20MHz,

TABLE 5: Sensor characteristics

Parameter	Symbol	Rating			Unit	Test Condition
		Min	Typ	Max		
Magnetic field range	FS	10		1000	mT	VCC=5V
Magnetic sensitivity	S	200		1.1	V/T	Both axis
Sensitivity programming resolution	Sres		0.1%			All measurement ranges
Magnetic field sensitivity temperature drift	TCsens	-1%		1%		TA -40 to 125 °C
Magnetic field sensitivity drift compensation range		0		3400	ppm/°C	
Magnetic field sensitivity drift compensation resolution			100		ppm/°C	
Output RMS noise	Vn	5			mV_{RMS}	Full signal BW
Eq. magnetic noise	Bn	25			µTrms	For full bandwidth
Output bandwidth (3 dB)	BW		1		MHz	

8.3. Output Characteristics:

TABLE 6: Electrical output characteristics

Parameter	Symbol	Rating			Unit	Test Condition
		Min	Typ	Max		
VOUT Output voltage range	Vout		0.25	4.75	V	10 kO load; VCC=5V
VOUT Offset	Voffset		<25		mV	
Voltage Output quiescent	VOQ		2.0			No magnetic field
VREF Output voltage range	Vref		0	4.75	V	10 kO load; VCC=5V
VREF Quiescent output resolution			40		mV	
VOQ fine adjustment range			-127	127	mV	
VOQ fine adjustment resolution			1		mV	
VOQ offset drift temperature compensation range			-2000	2000	µV/°C	
VOQ offset drift temperature compensation resolution			15.8		µV/°C	
Step Response time			1		µs	Delay between 90% input signal and 90 % output signal
Rise time			1		µs	
Fall time			1		µs	
Power on delay			400		µs	

8.4. Digital Interface Characteristics – Manchester, Single Wire:

TABLE 7: Digital interface characteristics

Parameter	Symbol	Rating			Unit	Test Condition
		Min	Typ	Max		
Data rate			Fosc/512	Fosc/10	bit/s	VCC=5V; on-chip oscillator 20 MHz
Min. delay between commands[1]			25.6		µs	VCC=5V; on-chip oscillator 20 MHz
Input high voltage	VIH		VCC-0.3	VCC+0.3	V	
Input low voltage	VIL		-0.3	0.3	V	

9. RECOMMENDED APPLICATION DIAGRAM

Item	Description	Value	Unit
C1	Bypass/Decoupling capacitor	100	nF

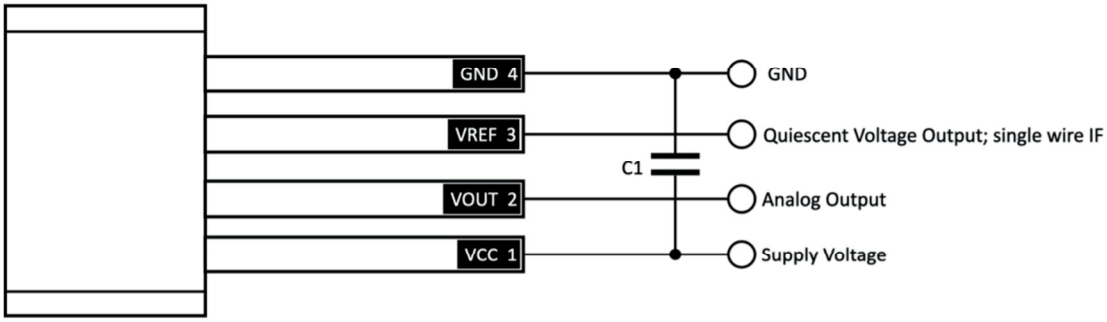


Figure 6: Application diagram

10. SINGLE WIRE INTERFACE

To activate the communication interface, the user needs to raise the supply voltage VCC to min. 6V. If activated, there are three operation modes available by sending a 32-bit command through the VREF pin:

- **Register access mode** – the user can directly read/write registers and change the sensor behavior
- **OTP programming mode** – once the preferred parameters are found and the user wants to select them, this more allows to write parameters to the OTP memory; also reading the entire OTP memory is done in this mode
- **Normal operation mode** – default mode after

power-on reset The three operation modes are

detailed in section 11.

The sensor IC uses a point-to-point protocol based on Manchester code according to G.E. Thomas' convention (rising edge within the bit boundary indicates '1' and a fallowing edge '0'; see Figure 2)

Convention according to G.E. Thomas:
- '0' is expressed as a mid-point high-to-low transition, '1' as low-to-high transition
- Encoded Output = Data XOR Clock

Note that this convention is inverse to the IEEE 802.3 convention.

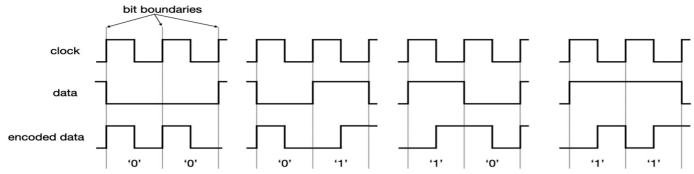


Figure 9: Manchester encoded interface according to G.E. Thomas

The MSB is sent first, and the host is supposed to release the drive on VREF if it expects a response from the sensor. Depending on the command, the response can be immediately or delayed by a few ms (for OTP fuse programming).Using the synchronization headers (characters 0x55 sent with each command and response) the device acquires the average bit period from the data stream, and uses it to decode the incoming data as well as to send back the response.

11. OPERATION MODES

11.1. NORMAL MODE

Command code: 0x5555 137F

This is the default mode after power-on. This command is used to return to normal operation after programming internal registers or reading/writing the OTP.

11.2. REGISTER ACCESS MODE

Command code: 0x5555 F731

In this mode, the user can read and write into the internal registers by sending additional commands through the Ref pin using half duplex communication (as defined below).

TABLE 8: Register read/write command

Command	Sync	Cde code	Register address	Expected answer	Response delay
Register read	0x55AA	0x6C	6 bits (MSB first)	0x556C followed by 8 data bits (MSB	After 8 bit-periods

Command	Sync	Cde code	Register address	Data	Expected answer	Response delay
Register write	0x55AA	0x6C	6 bits (MSB first)	8 bits (MSB first)	0x55C6first	After 8 bit-periods

11.3. PROGRAMMING MODE

Command code: 0x5555 31F7

In this mode, the user can program a single OTP memory fuse (bit), by selecting one of the 4x128 possibilities through a bit address. It is under user responsibility to ensure OTP consistency, by making sure that there is a valid configuration page associated with the valid checksum.

Command	Sync	Cde code	Prog. current	Fuse index	Expected answer	Response delay
OTP fuse/ write one bit	0x55AA	0xE1	2 bits Range [0:3]	9 bits Range [0:511]	0x55E1 When done	Tbd (ms)

Another command is used to read back the entire OTP memory.

Command	Sync	Cde code	Page Index 3 bits	Read Condition 2 bits	Expected answer	Response delay
OTP fuse/ write one bit	0x55AA	0xE1	000-011= User page 1XX=Factory page	'00': normal read '01': high -stress level read '10': low -stress level read '11': invalid	0x551E followed by 88bits	After 8 bit-periods

12. REGISTERS

12.1. INTERNAL REGISTER MAP

Table 10 shows the map of the internal registers including if values are loaded from OTP and the corresponding default values after power-on.

TABLE 9: Overview register map and default values

Command	Addr	Mode	Default	Meaning	OTP location	Factory/User calibration
SENS_COARSE	0x00	R/W	0x04	Measurement range selection	Yes	User
SENS_FINE	0x01	R/W	0x80	Hall element sensitivity adjustment	Yes	User
SENS_TC	0x02	R/W	0x00	Sensitivity temperature coefficient adjustment	Yes	User
VOQ_COARSE	0x03	R/W	0x32	Adjust and select quiescent output voltage (VREF); 40mV/step	Yes	User
VOQ_FINE	0x04	R/W	0x00	Quiescent output voltage (VREF) adjustment; 1mV/step	Yes	User
VOQ_TC	0x05	R/W	0x00	Quiescent output voltage temperature coefficient adjustment	Yes	User
SERIAL_ID	0x06 0x07 0x08	R/W	0x00	User defined serial number	Yes	User
Unused	0x09 to 0x0F	R/W	0x00	Unused	No	-
GLOBAL_CFG	0x10	R/W	0x00	Select: vertical/horizontal sensitivity axis; internal/external coil; fixed/ratiometric output; field polarities	Yes	Factory
HALL_CFG	0x11	R/W	0x11	Hall element spinning current configuration	Yes	Factory
HALL_BIAS_DAC	0x12	R/W	0x70	Hall bias current adjustment	Yes	Factory
COIL_CFG	0x13	R/W	0x77	Gain adjustment of coil signal path	Yes	Factory
FILTER_CFG	0x14	R/W	0x61	Select low-pass corner frequency; enable/disable coil path and high-pass filter; gain temperature coefficient adjustment	Yes	Factory
CLOCK_CAL	0x15	R/W	0x80	Oscillator frequency adjustment	Yes	Factory
CLOCK_TC	0x16	R/W		Oscillator temperature compensation	Yes	
LOT_ID	0x17 0x18	R/W	0x00	Factory defined lot number	Yes	Factory
Unused	0x19 to 0x1F	R/W	0x00	Unused	No	-
STATUS	0x20	R	0x1A or 0x0A	Reflects OTP status	No	-
TEST	0x11	R/W	0x0	Do not change; for internal use	No	Factory

12.2. DETAILED REGISTER CONTENT

The following subsections group the register content and provide detailed information about the contents.

12.2.1 Sensitivity/Gain Settings

Using the SENS_COARSE register, the user can select the measurement range from 5mT to 1T within 32 groups. For fine tuning a chosen range, the user can use the SENS_FINE register to adjust the gain up to +/-20% in 0.15% steps.

TABLE 10: Registers for sensitivity adjustment of the Hall sensor signal path

Register ID	Addr	Mode	Bits	Meaning	Default
SENS_COARSE	0x00	R/W	2:0	Gain setting within group defined by bit 4:3 0 1 2 3 4 5 6 7 0: 5.00, 5.94, 7.06, 8.39, 10.0, 11.9, 14.1, 16.7 1: 19.9, 23.7, 28.1, 33.4, 39.7, 47.2, 56.1, 66.7 2: 79.2, 94.2, 112, 133, 158, 188, 223, 265 3: 315, 375, 446, 530, 629, 748, 889, 1060	0x0
			4:3	Full scale output (2.5V bipolar or ratiometric). Each of these gain setting requires a different coil and calibration 0: 16.7mT 1: 66.7mT 2: 265mT 3: 1050mT	0x1
			5:6	Add 1700ppm/°C to SENS_TC low:high temp.	0x00
			7	Reserved	0x0
SENS_FINE	0x01	R/W	7-0	80->120%, 0.15%/step	0x80

For fine tuning a chosen range, the user can use the SENS_FINE register to adjust the gain up to
+/-5% in 0.15% steps. Using the SENS_COARSE register, the user can select the measurement range from 5mT to 1T within 32 groups.

TABLE 11: : Registers for gain setting – fine sensitivity of the Coil signal path

Register ID	Addr	Mode	Bits	Meaning	Default
COIL_CFG	0x13	R/W	7:0	Gain adjustment 0.0105dB/step, -6dB -> 10dB Note: The coil amplifier overall gain is controlled by the SENS_COARSE register. This register is used to match the gain of the Hall cell.	0x7

13.2.1 Sensor Temperature Compensation:

The Hall sensor signal is temperature dependent, thus it needs to be compensated. The temperature compensation circuit can be programmed in two segments. The switch-over threshold value can be selected between (20, 40, 60 and 80°C), using the GLOBAL_CFG[7:5] register.

TABLE 12: Registers temperature drift compensation of Hall elements

Register ID	Addr	Mode	Bits	Meaning	Default
SENS_TC	0x02	R/W	3-0	SENS_TC1: Add Bias current to compensate for temperature effect on sensitivity Iout= Iin *(1+ sens_tc1*50e-6 *(Tj-Thres)) This compensation is used for temperature **smaller** than threshold	0x0
			7:4	SENS_TC2: Add Bias current to compensate for temperature effect on sensitivity Iout= Iin *(1+ sens_tc2*50e-6 *(Tj-Thres)) This compensation is used for temperature **greater** than threshold	0x0

13.2.2 Quiescent Output settings:

The quiescent output (VREF) allows the differential measurement of the output signal (VOUT). The quiescent output voltage can adjusted to any value between 0V and VCC. However, the best performance is achieved when it is set within 0.5V of the power supply rail. The user can also select VOUT directly to be VCC/2. Thus, the output signal can be used in single-ended mode or differential mode. To cancel the residual offset due to imperfections in the signal chain, two registers are provided to compensate the offset and offset drift (Figure 10).

TABLE 13: Registers temperature drift compensation of Hall elements

Register ID	Addr	Mode	Bits	Meaning	Default
VOQ_COARSE	0x03	R/W	6:0	0V-5V max, 40mV/step	0x20
			7	Selection DAC or VCC/2	'0'
VOQ_FINE	0x04	R/W	6:0	127mV max, 1mV/step	0x0
			7	Polarity	'0'
VOQ_COARSE	0x05	R/W	6:0	2mV/C max, 15.8uV/C per step	0x0
			7	Polarity	'0'

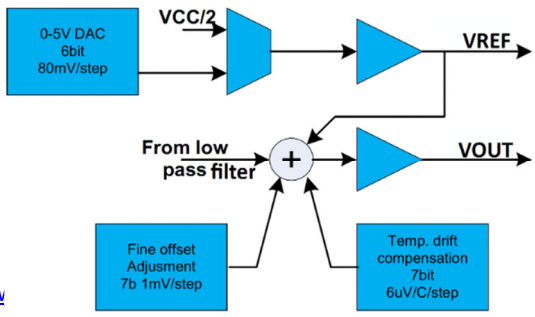


Figure 10: Signal path for VREF and VOUT

13.2.3 Coil, Hall Element Polarity and Filter Settings

The selection of coil polarity and vertical/horizontal sensitivity and ratiometric output or not is done through GLOBAL_CFG register.

TABLE 14: Registers for global settings

Register ID	Addr	Mode	Bits	Meaning	Default
GLOBAL_CFG	0x10	R/W	0	Hall sensor Horizontal/Vertical '0': Horizontal '1': Vertical	'0'
			1	Coil Internal/External '0': Internal '1': External	'0'
			2	Fixed gain/ ratiometric '0': Fixed gain '1': Ratiometric	'0'
			3	Hall Magnetic field polarity '0': Field enters IC, '1'->Reverse polarity	'0'
			4	Coil Magnetic field polarity '0': Field enters IC, '1'->Reverse polarity	'0'
			7-5	Temperature threshold calibration	'000'

13.2.4 Hall element configuration

TABLE 15: Register HALL_CFG settings

Register ID	Addr	Mode	Bits	Meaning	Default
HALL_CFG	0x11	R/W	1:0	Spinning Period '00', '01', '10' and '11' -> 200ns, 400ns, 600ns and 800ns	'01'
			2	Low noise amplifier reset pulse width '0'-> 50ns, '1'-> 100ns	'0'
			3	Rectifier Integration pulse width '0'-> 50ns, '1'-> 100ns	'0'
			4	Mask the measurement cycle for 1 clock (50ns) 0, 1 -> mask, no mask	'1'
			5	Fast mode where is each integrated into output '0' -> Normal, '1' -> Fast	'0'
			7:6	Unused	'00'

13.2.5 Hall bias setting

14. The bias current is proportional to clock frequency and reference voltage.

TABLE 16: Register HALL_BIAS_DAC settings

Register ID	Addr	Mode	Bits	Meaning	Default
HALL_BIAS_DAC	0x12	R/W	7:0	250u->4.25m; 15uA/step	0x70

14.1.1 Filter configuration

TABLE 17: Register FILTER_CFG settings

Register ID	Addr	Mode	Bits	Meaning	Default
FILTER_CFG	0x14	R/W	1:0	Low -pass filter corner frequency selection: '00': 5k, '01':10k, '10':20k	'01'
			2	'1': Enable 160k low pass for Hall sensor	'0'
			3	'1': Disable Coil path	'0'
			4	'1': Disable Coil high pass	'0'
			6:5	High pass selection 0:25/50/100 (for 5k,10k and 20k lp selection) 1:50/100/200 2:100/200/400 3:200/400/800	'3'

14.1.2 Oscillator clock trimming Sensitivity/Gain Settings

The oscillator needs to be adjusted to a frequency of 20 MHz ± 50 kHz to ensure that the filter corner frequencies are at the expected value.

TABLE 18: Register CLOCK_CAL settings for oscillator calibration/trimming

Register ID	Addr	Mode	Bits	Meaning	Default
CLOCK_CAL	0x15		7:0	8-32MHz, 100kHz/step	0x80
CLOCK_TC	0x16		3:0	-40 to 40°C range. Bit 3 controls the sign of the compensation and bits 2:0 control the temperature compensation in 7 steps of 100ppm	0xAA
			7:4	40°C and up. Bit 7 controls the sign of the compensation and bits 6:4 control the temperature compensation in 7 steps of 100ppm	

Status register

The (OTP) STATUS register bares information about the validity of OTP memory entries. Additionally, the TEMP_CAL bit indicates if the actual sensor temperature is beyond the temperature threshold which is adjusted using the three MSB bits in the FILTER_CFG[7:5] register (see Table 18). Note that this register is updated only after power-on except for the TEMP_CAL bit which is updated at run-time.

TABLE 19: Register for OTP status.

Register ID	Addr	Mode	Bits	Meaning	Default
STATUS	0x20	R	0	OTP factory parameters valid	
			1	OTP factory parameters checksum valid	
			2	OTP valid user page found	
			3	OTP user page checksum valid	
			4	TEMP_CAL	'0'/'1'[3]
			7:5	Reserved	'000'

12.3. OTP Memory Map

The OTP bit address is calculated by: <page> x 128 + <byte address> x 8 + <bit address>
Table 21 shows an overview of the OTP memory map. A page is considered valid only if the value of register PAGE_VALID equals 0xA5 and the checksum at byte address 0xF is correct. The valid checksum is calculated by the sum of all bytes within the range of one data set. For instance, the first user data set at page 0 reaches from byte address 0x0 to 0xA including the checksum. The sum of these bytes should result in 0. Thus, the checksum is the 2's complement sum all data bytes stored within this range.

TABLE 20: OTP memory map

	OTP bit address = <page> x 128 + <Byte address> x 8 + <Bit address>				
Parameters Type	OTP IP Block	Byte address	Page Index	Bit address 7-0	
User	0	0	User Page 0	SENS_Coarse	
		1		SENS_Fine	
		2		SENS_TC	
		3		VOQ_Coarse	
		4		VOQ_Fine	
		5		VOQ_TC	
		6		SERIAL_ID1	
		7		SERIAL_ID2	
		8		SERIAL_ID3	
		9		PAGE_VALID	A5 = valid, any other value means invalid
		A		CHECKSUM	Sum of all bytes including checksum should be 0. If not, page declared invalid.
		B	User Page 1	SENS_Coarse	And associated register keep reset value.
		C		SENS_Fine	
		D		SENS_TC	
		E		VOQ_Coarse	
		F		VOQ_Fine	
	1	0		VOQ_TC	
		1		SERIAL_ID1	
		2		SERIAL_ID2	
		3		SERIAL_ID3	
		4		PAGE_VALID	A5 = valid, any other value means invalid
		5		CHECKSUM	Sum of all bytes including checksum should be 0. If not, page declared invalid.
		6	User Page 2	SENS_Coarse	And associated register keep reset value.
		7		SENS_Fine	
		8		SENS_TC	
		9		VOQ_Coarse	
		A		VOQ_Fine	
		B		VOQ_TC	
		C		SERIAL_ID1	
		D		SERIAL_ID2	
		E		SERIAL_ID3	
		F		PAGE_VALID	A5 = valid, any other value means invalid
	2	0		CHECKSUM	Sum of all bytes including checksum should be 0. If not, page declared invalid.
		1	User Page 3	SENS_Coarse	And associated register keep reset value.
		2		SENS_Fine	
		3		SENS_TC	
		4		VOQ_Coarse	
		5		VOQ_Fine	
		6		VOQ_TC	
		7		SERIAL_ID1	
		8		SERIAL_ID2	
		9		SERIAL_ID3	
		A		PAGE_VALID	A5 = valid, any other value means invalid
		B		CHECKSUM	Sum of all bytes including checksum should be 0. If not, page declared invalid.
		C		Unused	And associated register keep reset value.
		D		Unused	
		E		Unused	
		F		Unused	
Factory	3	0	Factory Page	GLOBAL_CFG	
		1		HALL_CFG	
		2		HALL_BIAS_DAC	
		3		COIL_CFG	
		4		FILTER_CFG	
		5		CLOCK_CAL	
		6		CLOCK_TC	
		7		LOT_ID1	
		8		LOT_ID2	
		9		PAGE VALID	A5 = valid, any other value means invalid
		A		CHECKSUM	Sum of all bytes including checksum should be 0. If not, page declared invalid.
		B		Unused	And associated register keep reset value.
		C		Unused	
		D		Unused	
		E		Unused	
		0		Unused	